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EXAMINER	
KING, JUSTIN	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/819,996	BENNETT ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17, 19-27, and 30* is/are rejected.

7)☒ Claim(s) *18,28 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040822*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 15 recites the limitation "said control device" in the last limitation. There is insufficient antecedent basis for this limitation in the claim. Claims 16-20 are rejected because they incorporate claim 15's limitations.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Neal et al. (U.S. Patent No. 5,774,706).

Referring to claims 1 and 21: Neal discloses that a ground pin is utilized in the PCI bus to determine the bus operating frequency (column 2, lines 12-24). A memory component, such as a hard drive, is included in each computer system; thus, the data fetching from the hard drive based on the determination on whether the ground pin is

grounded is the claimed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**. Hence, claim is anticipated by Neal.

5. Claims 1, 3, 21, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Kelley et al. (U.S. Patent No. 6,295,568).

Referring to claims 1 and 21: Kelley discloses a system supporting multiple frequencies. Kelly discloses that a memory component, such as the PCI hard drive, is well-known in a computer system (column 1, lines 34-36). Kelly further discloses a frequency control logic, which determines the frequency by polling the PCI peripheral component slots; such polling is the clamed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**. Hence, claim is anticipated by Kelley.

Referring to claim 3: Kelly further discloses that the lower PCI frequency (33 MHz) supports four peripheral devices while the higher PCI frequency (66 MHz) only supports two peripheral devices (column 1, lines 45-49). Thus, the Kelly discloses that the parameters further relate to a threshold value.

Referring to claim 24: Claims 1 and 21's arguments apply; furthermore, Kelley discloses the parameter set (clock speed, column 1, line 62, loading effect, column 4, 1st paragraph) from a plurality of parameter sets.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 2, 4, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Neal and Avery et al. (U.S. Patent No. 5,577,213).

Referring to claims 2 and 25: Neal's disclosure is stated above; Neal does not explicitly disclose data transfer size. Avery discloses a customized interface between the bus and peripheral device, which the interface accepts the parameters for configuration. Avery teaches one to configure the buffers in different sizes (column 10, lines 6-12). Thus, it would have been obvious to one having ordinary skill in the computer art to adapt Avery's teaching onto Neal because Avery teaches one to enable a bus to accommodate dissimilar devices by setting different parameters.

Referring to claim 4: Neal's disclosure is stated above; Neal discloses the obtaining parameters corresponding to the bus frequency, but Neal does not explicitly

disclose register for storing values. Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1).

9. Claims 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Neal and Avery.

Referring to claim 3: Neal does not explicitly disclose any threshold value. Avery disclosed the different buffer widths (column 10, line 10), which are the threshold values. Thus, it would have been obvious to one having ordinary skill in the computer art to adapt Avery's teaching onto Neal because Avery teaches one to enable a bus to accommodate dissimilar devices by setting different parameters.

10. Claims 2, 4, 7-9, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the combination of Kelley and Avery.

Referring to claims 2 and 25: Kelley's disclosure is stated above; Kelley does not explicitly disclose data transfer size. Avery discloses a customized interface between the bus and peripheral device, which the interface accepts the parameters for configuration. Avery teaches one to configure the buffers in different sizes (column 10, lines 6-12). Thus, it would have been obvious to one having ordinary skill in the computer art to adapt Avery's teaching onto Kelley because Avery teaches one to enable a bus to accommodate dissimilar devices by setting different parameters.

Referring to claim 4: Kelley's disclosure is stated above; Kelley discloses the obtaining parameters corresponding to the bus frequency, but Kelley does not explicitly

disclose register for storing values. Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1).

Referring to claim 7: Kelley discloses a system supporting multiple frequencies. Kelly discloses that a memory component, such as the PCI hard drive, is well-known in a computer system (column 1, lines 34-36). Kelly further discloses a frequency control logic, which determines the frequency by polling the PCI peripheral component slots; the control logic is the clamed **control unit to receive an indication regarding a frequency of a bus.**

Kelley does not explicitly disclose registers for storing values. Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1). . Avery teaches one to configure the buffers in different sizes (column 10, lines 6-12). Thus, it would have been obvious to one having ordinary skill in the computer art to adapt Avery's teaching onto Kelley because Avery teaches one to enable a bus to accommodate dissimilar devices by setting different parameters.

Referring to claim 8: Avery discloses a customized interface between the bus and peripheral device, which the interface accepts the parameters for configuration. Avery teaches one to configure the buffers in different sizes (column 10, lines 6-12).

Referring to claim 9: Kelly discloses that the lower PCI frequency (33 MHz) supports four peripheral devices while the higher PCI frequency (66 MHz) only supports two peripheral devices (column 1, lines 45-49). Thus, the Kelly discloses that the parameters further relate to a threshold value. Avery also disclosed the different buffer widths (column 10, line 10), which are the threshold values.

11. Claims 5-6, 12-14, 22-23, 26-27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Chambers et al. (U.S. Patent No. 6,289,406) and Kelley.

Referring to claim 5: Chambers discloses a bridge with a memory component (figure 4, structure 330 or structure 322) and a storage device (figure 4, structure 330 or structure 322). Chambers discloses asserting access request (figure 6, step 505), which is the claimed fetching an initial amount of data from said memory component and storing said initial amount of data in a storage device. Chambers further discloses forwarding data with latency (figure 6, steps 521-540), which is the claimed fetching-additional data from said memory component at least based on a threshold value of said storage device.

Chambers does not explicitly disclose obtaining parameters and the threshold values relating to bus frequencies. Kelley discloses a system supporting multiple frequencies. Kelly discloses that a memory component, such as the PCI hard drive, is well-known in a computer system (column 1, lines 34-36). Kelly further discloses a frequency control logic, which determines the frequency by polling the PCI peripheral component slots; such polling is the clamed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**. Kelly further discloses that the lower PCI frequency (33 MHz) supports four peripheral devices while the higher PCI frequency (66 MHz) only supports two peripheral devices (column 1, lines 45-49). Thus, the Kelly discloses that the parameters further relate to a threshold value. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made

the invention to adapt Kelley's teaching onto Chambers because Kelley teaches one to dynamically adjust the bus frequency to optimize the bus performance.

Referring to claim 6: Chambers discloses fetching said data further comprises starting a timer, and fetching additional data from said memory component when said timer has elapsed (figure 4, structure 324).

Referring to claim 12: Chambers discloses fetching a size of data from a memory subsystem on one side of a host chipset (figure 4, structure 306) for a bus device on an opposite side of said host chipset as a function of said frequency of said bus.

Referring to claim 13: Chambers discloses a primary bus and a secondary bus (figure 4, structures 310 and 312).

Referring to claim 14: Chambers discloses the bus as PCI bus and the chip-set as the PCI bridge. Kelley discloses a PCI-to-PCI bridge (figure 3, structure 76, abstract).

Referring to claim 22: Chambers discloses a bridge with a memory component (figure 4, structure 330 or structure 322) and a storage device (figure 4, structure 330 or structure 322). Chambers discloses asserting access request (figure 6, step 505), which is the claimed fetching an initial amount of data from said memory component and storing said initial amount of data in a storage device. Chambers further discloses forwarding data with latency (figure 6, steps 521-540), which is the claimed fetching-additional data from said memory component at least based on a threshold value of said storage device.

Chambers does not explicitly disclose obtaining parameters and the threshold values relating to bus frequencies. Kelley discloses a system supporting multiple frequencies. Kelly discloses that a memory component, such as the PCI hard drive, is well-known in a computer system (column 1, lines 34-36). Kelly further discloses a

frequency control logic, which determines the frequency by polling the PCI peripheral component slots; such polling is the clamed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**. Kelly further discloses that the lower PCI frequency (33 MHz) supports four peripheral devices while the higher PCI frequency (66 MHz) only supports two peripheral devices (column 1, lines 45-49). Thus, the Kelly discloses that the parameters further relate to a threshold value. Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Kelley's teaching onto Chambers because Kelley teaches one to dynamically adjust the bus frequency to optimize the bus performance.

Referring to claim 23: Chambers discloses fetching said data further comprises starting a timer, and fetching additional data from said memory component when said timer has elapsed (figure 4, structure 324).

Referring to claims 26-27: Chambers discloses fetching comprises issuing a request to transfer data from the memory component to a buffer, and then issuing another request in response to the threshold value and a data amount comprising data stored in the buffer indicating that more data needs to be fetched to maintain a stream of data between the buffer and a device (figure 4, structures 322, 324, and 330). Kelly further discloses that the lower PCI frequency (33 MHz) supports four peripheral devices while the higher PCI frequency (66 MHz) only supports two peripheral devices (column 1, lines 45-49). Thus, the Kelly discloses that the parameters further relate to a threshold value.

Referring to claim 30: Chambers discloses fetching said data further comprises starting a timer, and fetching additional data from said memory component when said timer has elapsed (figure 4, structure 324).

12. Claims 10-11, 15-17, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Chambers in view of Kelley, and in further view of Avery.

Referring to claim 10: Chambers discloses a bridge with a memory component (figure 4, structure 330 or structure 322) and a storage device (figure 4, structure 330 or structure 322). Chambers discloses asserting access request (figure 6, step 505), which is the claimed fetching an initial amount of data from said memory component and storing said initial amount of data in a storage device. Chambers further discloses forwarding data with latency (figure 6, steps 521-540), which is the claimed fetching-additional data from said memory component at least based on a threshold value of said storage device.

Chambers does not explicitly disclose obtaining parameters and the threshold values relating to bus frequencies. Kelley discloses a system supporting multiple frequencies. Kelly discloses that a memory component, such as the PCI hard drive, is well-known in a computer system (column 1, lines 34-36). Kelly further discloses a frequency control logic, which determines the frequency by polling the PCI peripheral component slots; the control logic is the clamed **control unit to receive an indication regarding a frequency of a bus.**

Chambers does not explicitly disclose registers for storing values. Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1). Avery teaches one to configure the buffers in different sizes (column 10, lines

6-12). Thus, it would have been obvious to one having ordinary skill in the computer art to adapt Avery's teaching onto Kelley because Avery teaches one to enable a bus to accommodate dissimilar devices by setting different parameters.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Kelley's teaching onto Chambers because Kelley teaches one to dynamically adjust the bus frequency to optimize the bus performance.

Referring to claim 11: Chambers discloses fetching said data further comprises starting a timer, and fetching additional data from said memory component when said timer has elapsed (figure 4, structure 324).

Referring to claim 15: Chambers discloses a memory subsystem (figure 4, structure 304), host chipset (figure 4, structure 306) couple to the memory subsystem via a first bus (figure 4, structure 310), and a bus device (figure 4, structure 330) to couple to said host chipset via a second bus (figure 4, structure 312). Chambers further discloses that the host chipset fetches data from said memory subsystem for said bus device upon request (figure 6), said host chipset comprising, a buffer device (figure 4, structure 322) to store data fetched from said memory subsystem via said first bus for said bus device.

Chambers does not explicitly disclose a plurality of registers each to contain parameters corresponding to a different operating frequency of said second bus and a data fetching mechanism to receive an indication of an operating frequency of said second bus and to obtain said parameters corresponding to said operating frequency of said second bus based on said indication, fetch said data from said memory component based on said obtained parameters.

Kelley discloses a system supporting multiple frequencies. Kelly discloses that a memory component, such as the PCI hard drive, is well-known in a computer system (column 1, lines 34-36). Kelly further discloses a frequency control logic, which determines the frequency by polling the PCI peripheral component slots; such polling is the clamed **obtaining parameters relating data fetching from said memory component based on an operating frequency of a bus.** And the actual data fetching is the claimed **fetching said data from said memory component based on said obtained parameters**.

Chambers does not explicitly disclose registers for storing values. Avery discloses registers for storing the parameters/configuration information (column 15-16, table 1). Avery teaches one to configure the buffers in different sizes (column 10, lines 6-12). Thus, it would have been obvious to one having ordinary skill in the computer art to adapt Avery's teaching onto Kelley because Avery teaches one to enable a bus to accommodate dissimilar devices by setting different parameters.

Hence, it would have been obvious to one having ordinary skill in the computer art at the time Applicant made the invention to adapt Kelley's teaching onto Chambers because Kelley teaches one to dynamically adjust the bus frequency to optimize the bus performance.

Referring to claim 16: Chambers discloses a PCI bridge, and the PCI standard specifies it to be either 32 or 64 bit (Application, page 1, last line).

Referring to claim 17: Kelley discloses a PCI-to-PCI bridge (figure 3, structure 76, abstract).

Referring to claim 19: Chambers discloses asserting access request (figure 6, step 505), which is the claimed fetching an initial amount of data from said memory component and storing said initial amount of data in a storage device. Chambers further discloses forwarding data with latency (figure 6, steps 521-540), which is the claimed fetching-additional data from said memory component at least based on a threshold value of said storage device.

Referring to claim 20: Chambers discloses fetching said data further comprises starting a timer, and fetching additional data from said memory component when said timer has elapsed (figure 4, structure 324).

Allowable Subject Matter

13. Claims 18 and 28-29 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Referring to claim 18: The prior arts on record do not disclose or explicitly teach initial request length, initial threshold length, subsequent request length, and subsequent threshold length as the parameters relating to data fetching based on the operating frequency of the bus.

Referring to claim 28: The prior arts on record do not disclose or explicitly teach that each parameters set includes a first data transfer size and a second data transfer size, and system fetches a first request to request data having the first data transfer size and issues the second request to request data having the second data transfer size.

Referring to claim 29: The prior arts on record do not disclose or explicitly teach that each parameter set includes a first data transfer size, a second data transfer size, a first threshold value, and a second thresh based upon corresponding operating characteristics of the bus. The prior arts on record also do not disclose or explicitly teach that fetching a first request to transfer data having the first data transfer size from the memory component to a buffer, issuing a second request to transfer data having the second data transfer size from the memory component to the buffer.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 703-305-4571. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-308-3110. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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Justin King
August 26, 2004